

Sabt A

WHAT IS CLAIMED IS:

1 1. A die seal structure for a semiconductor die having a substrate
2 comprising:
3 an elongate region electrically isolated from the remainder of the substrate
4 extending around a major portion of the periphery of the substrate and having a gap
5 between ends of the elongate region along a minor portion of the periphery; and
6 a conductive seal ring extending around the entire periphery of the die in
7 contact with the die at said elongate region and said gap to provide a limited electrical
8 connection between the ring and the substrate at said gap.

1 2. The structure of claim 1 wherein the substrate has a first
2 conductivity type, and wherein the elongate region comprises an elongate well region of a
3 second conductivity type different from the conductivity of the first conductivity type.

1 3. The structure of claim 2 wherein the first conductivity type is p-
2 type and the second conductivity type is n-type.

1 4. The structure of claim 2 wherein the first conductivity type is n-
2 type and the second conductivity type is p-type.

1 5. The structure of claim 1 wherein the elongate region comprises an
2 elongate dielectric region between the seal ring and the substrate.

1 6. The structure of claim 1 wherein the seal ring only electrically
2 contacts the substrate of the semiconductor die at the gap.

1 7. The structure of claim 1 wherein the substrate is formed of silicon.

1 8. The structure of claim 1 wherein the conductive seal ring
2 comprises a multilayer structure of alternating conducting and insulating layers, and
3 wherein vias are formed in the insulating layers.

1 9. A method of sealing a semiconductor die having a substrate of a
2 first conductivity type, comprising:
3 forming an elongate well region of a second conductivity type opposite
4 from the first conductivity type extending around a major portion of the periphery of the

5 substrate and having a gap between ends of the well region at a minor portion of the
6 periphery; and

7 placing a conductive seal ring extending around the entire periphery of the
8 die in contact with said well region and said gap to provide limited electrical contact
9 between the ring and the substrate of said first conductivity type at said gap.

10. The method of claim 9 wherein the substrate of the semiconductor
1 die has an n-type conductivity and wherein said forming an elongate well region of a
2 second conductivity type step includes forming an elongate well region of a p-type
3 conductivity.

11. The method of claim 9 wherein the substrate of the semiconductor
2 die an n-type conductivity and wherein said forming an elongate well region of a second
3 conductivity type step includes forming an elongate well region of a p-type conductivity.

12. The method of claim 9 wherein the substrate of the semiconductor
2 die is formed of silicon.

13. The method of claim 9 wherein said placing step includes
2 sequentially forming a multiplicity of alternating conductive and insulative layers
3 overlying one another, and forming vias in the insulating layers.

14. A die seal structure for a semiconductor die having a substrate of a
2 first conductivity type, comprising:

3 an elongate well region of a second conductivity type opposite from the
4 first conductivity type extending around a major portion of the periphery of the substrate
5 and having a gap between the ends of the elongate region along a minor portion of the
6 periphery; and

7 a conductive seal ring extending around the entire periphery of the die in
8 contact with the die at said elongate well region and said gap to provide a limited
9 electrical connection between the ring and the substrate of said first conductivity type at
10 said gap.

15. The structure of claim 14 wherein the first conductivity type is
2 p-type and the second conductivity type is n-type.

1 16. The structure of claim 14 wherein the first conductivity type is n
2 type and the second conductivity type is p type.

1 17. The structure of claim 14 wherein the conductive seal ring
2 comprises a multilayer structure of alternating conducting and insulating layers, and
3 wherein vias are formed in the insulating layers.
Subt a³

1 18. A semiconductor device comprising:
2 a. a die including a substrate;
3 b. a die seal structure on the substrate, the structure comprising:
4 an elongate region electrically isolated from the remainder of the
5 substrate extending around a major portion of the periphery of the substrate and having a
6 gap between ends of the elongate region along a minor portion of the periphery; and
7 a conductive seal ring extending around the entire periphery of the die in
8 contact with the die at said elongate region and said gap to provide a limited electrical
9 connection between the ring and the substrate at said gap.

1 19. The structure of claim 18 wherein the substrate has a first
2 conductivity type, and wherein the elongate region comprises an elongate well region of a
3 second conductivity type different from the conductivity of the first conductivity type.

1 20. The structure of claim 18 wherein the first conductivity type is p-
2 type and the second conductivity type is n-type.

1 21. The structure of claim 18 wherein the first conductivity type is n-
2 type and the second conductivity type is p-type.

1 22. The structure of claim 18 wherein the elongate region comprises an
2 elongate dielectric region between the seal ring and the substrate.

1 23. The structure of claim 18 wherein the seal ring only electrically
2 contacts the substrate of the semiconductor die at the gap.

1 24. The structure of claim 18 wherein the substrate is formed of
2 silicon.

1 25. The structure of claim 18 wherein the conductive seal ring
2 comprises a multilayer structure of alternating conducting and insulating layers, and
3 wherein vias are formed in the insulating layers.

1 26. The structure of claim 18 wherein the elongate region is isolated by
2 oxide.

1 27. The structure of claim 26 wherein the conductive seal ring is
2 connected to the substrate by a metal stub.

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